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EXAMINER	
DUONG, KHANH B	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/789,637	SCHIECK ET AL.	
	Examiner	Art Unit	
	KHANH B. DUONG	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,13,14,16-18 and 36-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7, 13, 14, 16-18 and 36-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 24, 2009 has been entered.

Response to Amendment

This office action is responsive to the amendment filed August 24, 2009.

Accordingly, claims 6, 8-12, 15 and 19-35 were canceled, claims 1, 7, 13, 16 and 17 were amended and new claims 36-40 were added.

Currently, claims 1-5, 7, 13, 14, 16-18 and 36-40 remain pending.

Response to Arguments

Applicant's arguments with respect to the amended and new claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

The indicated allowability of claims 2, 6, 7 and 15-17 is withdrawn in view of the newly discovered reference(s) to Han et al. (U.S. 6,429,532) and Magdo (U.S. 5,262,719). Rejections based on the newly cited and previously reference(s) follow.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "*package substrate includes a*

conductive trace disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within said package substrate and along said conductive trace" must be shown or the feature(s) canceled from the claims 13 and 38. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 13, 14, 16-18 and 38 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Re claim 13, the specification does not describe a package substrate comprising a conductive trace disposed such that "*multiple test signals are accessible at varying degrees of electronic component granularity within said package substrate and along said conductive trace*".

Re claim 38, the specification does not describe a "package substrate" comprising a conductive trace disposed such that "*test signals are accessible at varying degrees of electronic component granularity*".

*** Other claims are rejected as depending on the rejected base claim(s).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 13, 14, 16-18 and 36-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "said signal redistribution layer" in line 13. There is insufficient antecedent basis for this limitation in the claim.

Claim 36 recites the limitation "said signal redistribution layer" in line 10. There is insufficient antecedent basis for this limitation in the claim.

*** Other claims are rejected as depending on the rejected base claim(s).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 13, 14 and 16-18 rejected under 35 U.S.C. 102(b) as being anticipated by Motika et al. (U.S. 5,807,763).

Re claim 13, Motika et al. ("Motika") expressly discloses in FIG. 4 a semiconductor device comprising: a package substrate 240, wherein said package substrate 240 includes a conductive trace 244; and a semiconductor die 234 having test probe points (below probe 232), wherein said semiconductor die 234 is electrically coupled to said package substrate 240, wherein said semiconductor die 234 comprises: a conductive test signal bump, said conductive test signal bump 204 located on a first surface of said semiconductor die 234 and electrically coupled to a signal redistribution layer; a redistribution layer including a test signal redistribution layer trace, said signal redistribution layer communicatively coupled said conductive test signal bump; a test probe point (below probe 232); and a test access via (under bump 204).

The claim recites the following functional and intended use limitations: "*for communicating test signals on an external access point*", "*multiple test signals are accessible at varying degrees of electronic component granularity within said package substrate and along said conductive trace*", "*for transmitting internal test signals off of said semiconductor die to said package substrate*", "*test probe points accessible by said external access point*", "*for*

communicating internal signals to said conductive test signal bump", "*for accessing said test signals in said semiconductor die*", "*for electrical coupling to said signal redistribution layer*", and "*for electrically coupling said test probe point to said signal redistribution layer*". These limitations has not been given patentable weight because it is narrative in form. In order to be given patentable weight, a functional recitation must be expressed as a "means" for performing the specified function, as set forth 35 U.S.C. 112, 6th paragraph, and must be supported by recitation in the claim of sufficient structure to warrant the presence of the functional language. *In Re Fuller*, 1929 C.D. 172; 388 O.G. 279.

In addition, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963); *Ex parte Masham*, 2USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). In the instant case and as explained above, Motika shows all structural limitations specifically recited in the claim and it appears that the recited functional limitation does not affect the structure of Motika. Furthermore, labels, statements of intended use, or functional language do not structurally distinguish claims over prior art, which can function in the same manner, be labeled in the same manner, or be used in the same manner. See *MPEP 2112.01*.

Re claim 14, Motika expressly discloses in FIG. 4 said package substrate 240 comprises: a first surface with ball grid array; a second surface with conductive contacts for electrically coupling with conductive bumps of said semiconductor die 234; and a trace 244 for electrically coupling one of said conductive contacts to said external access point 252.

Re claim 16, Motika expressly shows in FIG. 1 said test probe point 140 comprises a "focused ion beam (FIB) pad". In addition, the claim recites the following functional language: "accessible by focused ion bean drilling and conductive material backfill". See discussion of claim 13 above regarding functional recitations.

Re claim 17, Motika expressly shows in FIG. 1 said test signal redistribution trace (126/134) is routed in patterns in which trace widths and spacing between redistribution layer traces (126/134) appear to be minimized without causing signal interference.

Re claim 18, Motika discloses said external access point 252 is accessible by automatic test equipment [see col. 7, lines 29-33].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han et al. (U.S. 6,429,532) in view of Magdo (U.S. 5,262,719).

Han et al. ("Han") discloses in FIG. 3 a semiconductor die comprising: a conductive test signal bump 204 for transmitting test signals off of said semiconductor die; a test signal redistribution layer trace 212 for communicating said test signals to said conductive test signal bump 204, wherein said test signal redistribution layer trace 212 is included in a redistribution layer, said test signal redistribution layer trace 212 communicatively coupled to said conductive test signal bump 204; and a test probe point 212a for accessing said test signals in said semiconductor die and for electrical coupling to said redistribution layer.

Re claim 1, Han does not disclose said test signal redistribution layer trace 212 is routed in a spiral pattern.

Magdo expressly shows in FIG. 5 a test signal redistribution layer trace (50/54/58) being routed in a spiral pattern for the purpose of maximizing the wiring (trace) area to provide meaningful process yield data [see col. 2, lines 37-41].

Since Han and Magdo are from the same field of endeavor, the purpose disclosed by Magdo would have been recognized in the pertinent prior art of Han.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the device of Han as suggested by Magdo because of the desirability to maximize the trace area to provide meaningful process yield data.

The claim recites the following functional and intended use limitations: "*said test signal redistribution trace is disposed such that multiple test signals are accessible at varying degrees of electronic component granularity within said die and along said test signal redistribution layer trace*". See discussion above of claim 13 regarding functional and intended use recitations.

Re claim 2, Han discloses in FIG. 3 said semiconductor die is a flip chip die [see col. 1, 5-9]. In addition, the claim recites the following functional and intended-use language: "*configured for connection to a package substrate such that said conductive test signal bump is electrically coupled to an external access point of said package substrate*". See discussion above of claim 13 regarding functional recitations.

Re claims 3-5, the claims also recite the following product-by-process limitations: "accessible by drilling" (claim 3); "a focused ion beam (FIB) pad accessible by focused ion beam drilling and conductive material backfill" (claim 4); and "conductive material backfill" (claim 5). However, these limitations have not been given patentable weight because product-by-process claims are not limited to the manipulations of the recited steps, only the structure implied by the steps. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698,

227 USPQ 964, 966 (Fed. Cir. 1985). Thus, Han expressly shows in FIG. 3 the test probe point 212a comprises a bonding pad which is coupled to said test signal redistribution layer, wherein the bonding pad is communicatively coupled to said test signal redistribution layer trace 212 by a conductive material backfill.

Re further claim 5, the claim also recites the following intended use language: "*wherein said test signal redistribution layer trace is dedicated for test signals*". See discussion above of claim 13 regarding intended use recitations.

Re claim 7, see discussion above regarding claim 1. Magdo further expressly shows in FIG. 5 said test signal redistribution layer trace (50/54/58) is routed in said spiral pattern with "conductive fingers" located in positions. In addition, the claim recites the following intended use languages: "*conductive fingers located in positions such that drilling and conductive material backfill provides access to internal signals for testing at various electronic component configuration granularity*". See discussion above of claim 13 regarding intended use recitations.

Claims 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika in view of Magdo (U.S. 5,262,719).

Motika discloses a semiconductor device previously as discussed above regarding claims 13, 14 and 16-18 which device is repeated herein.

Re claim 36, Motika does not disclose said test signal redistribution layer trace 212 is routed in a spiral pattern.

Magdo expressly shows in FIG. 5 a test signal redistribution layer trace (50/54/58) being routed in a spiral pattern for the purpose of maximizing the wiring (trace) area to provide meaningful process yield data [see col. 2, lines 37-41].

Since Motika and Magdo are from the same field of endeavor, the purpose disclosed by Magdo would have been recognized in the pertinent prior art of Motika.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the device of Motika as suggested by Magdo because of the desirability to maximize the trace area to provide meaningful process yield data.

The claim also recites the following functional and intended use limitations: "*for communicating test signals on an external access point*", "*accessible by said external access point*", "*for transmitting internal test signals off of said semiconductor die to said package substrate*", "*for communicating internal signals to said conductive test signal bump*", "*for accessing said test signals in said semiconductor die*", "*for electrical coupling to said signal redistribution layer*", and "*for electrically coupling said test probe point to said signal redistribution layer*". See discussions above of claim 13 regarding functional and intended use limitations.

Re claim 37, see discussion above regarding claim 36. Magdo further expressly shows in FIG. 5 said test signal redistribution layer trace (50/54/58) is routed in said spiral pattern with "conductive fingers" located in positions. In addition, the claim recites the following intended use languages: "*conductive fingers located in positions such that drilling and conductive material backfill provides access to internal signals for testing at various electronic component configuration granularity*". See discussion above of claim 13 regarding intended use recitations.

Re claim 38, Motika expressly discloses in FIG. 4 said package substrate 240 comprises a conductive trace 244.

Re claim 39, Motika expressly discloses in FIG. 4 said package substrate 240 comprises: a first surface with ball grid array 256; a second surface with conductive contacts 252 for electrically coupling with conductive bumps of said semiconductor die 234, including a conductive contact 252 for electrically coupling with a conductive test signal bump; and a trace 244 for electrically coupling one of said conductive contacts 252 to said external access point.

Re claim 40, Motika expressly discloses in FIG. 4 said test signal is a semiconductor die signal while said semiconductor die 234 is operating.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following U.S. patents teach devices for testing semiconductor die: Liu '853, Chang '369, Akagawa '844, Lee '294, Malladi '252, Yojima '744 and Hembree '524.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on Monday-Friday from 8:30-4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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